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EFFECTS OF GATE OXIDE SHORTS IN CMOS INVERTER CIRCUIT

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Abstract: Gate oxide shorts of MOS transistors play a key role to cause logic errors as well as to show unusual behaviour in CMOS logic gate operation. Although it is unintended electrical connections, but it acts as a dominant defect in some CMOS fabrication processes. By using a realistic model, logic operation of the inverter circuit has been evaluated by changing the resistance of the short, power supply and operating temperature. A dynamic circuit simulator (SPICE) provides the necessary data to verify the analysis considering oxide shorts for n- and p-channel transistors.

Key words: Gate oxide shorts; Inverter; Breakdown voltage; Realistic model

Introduction

In CMOS technology, both pMOS and nMOS transistors are employed to form the logic families. Gate oxide shorts between gate and source or drain or channel in CMOS fabrication process have been identified as an important type of fabrication fault (Hawkins, 1985) and major source of IC reliability problem. This problem had been modeled as gate-to-source and gate-to-drain shorts of MOS transistors assuming that no resistance was present in this short (Al-Arian and Agarwal, 1988; Rajsuman and Jayasumana, 1987). But ignoring of this resistance could result in misleading conclusion or strange circuit behaviour (Viswesswaran, 1991). Due to the different electrical properties of MOS transistors, gate oxide shorts should be properly modeled. In this paper, a realistic model in CMOS inverter has been implemented and shown that the circuit operation with gate oxide short is found to be extensively dependent on the resistance of the short, power supply and operating temperature.

Modeling of Gate Oxide Short

Possible gate oxide short types have been illustrated in Fig. 1. Basically, these shorts are caused either by defects in the gate oxide or by excessive voltage across the gate oxide (Soden and Hawkins, 1986). And the developed resistance depends on many factors such as defect size, oxide thickness, electrical conditions causing the breakdown (Hamdy, 1988).

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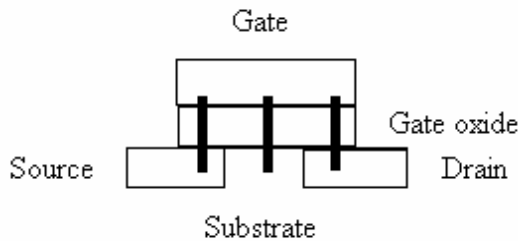


Fig. 1. Possible gate oxide shorts.

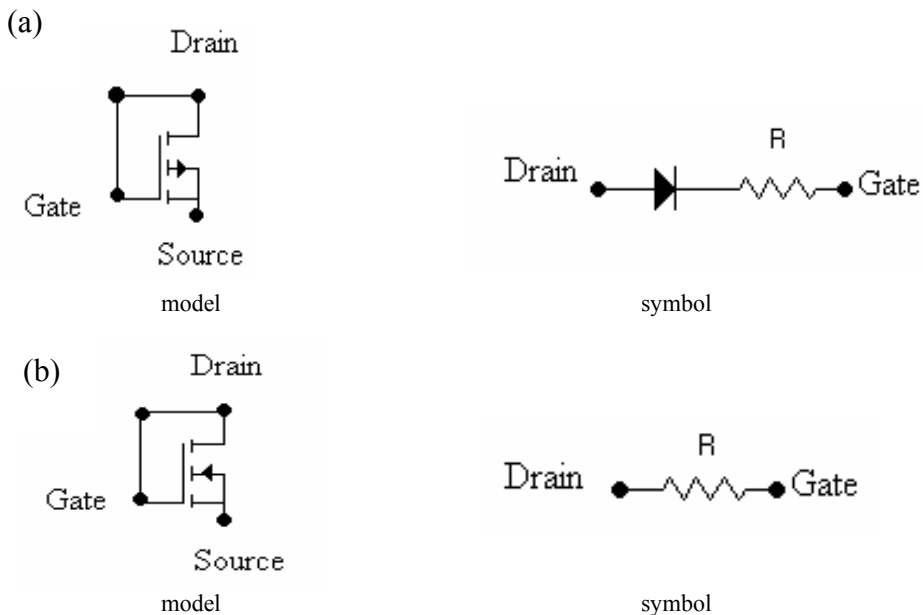


Fig. 2. Models and symbols for drain-to-gate shorts for (a) pMOS and (b) nMOS transistors.

Measured resistance of several shorts between the gate and source or drain in nMOS ranged between 0.8 and 4 K Ω (Soden and Hawkins, 1986). Fig. 2 shows the model and the corresponding symbols in such shorts. For gate-to-source and gate-to-drain shorts in n-channel transistors, resistive connections were observed and the electrical model is simply a resistor (Syrzycki, 1989). In p-channel transistor, this short forms a p-n junction diode in series with a resistor allowing current in both directions (Hao and McCluskey, 1993).

Operation of CMOS Inverter

The general arrangement of CMOS inverter is shown in Fig. 3. While analyzing the properties of logic operation using the more realistic model, one gate oxide short will be considered in one of the MOS transistors. Simultaneously, the analysis will be extended

for multiple shorts. SPICE simulation will be performed to verify the analysis using 0.8 μm CMOS process.

(i) Effect of resistance: The resistance of the gate oxide short plays a vital role in determining the circuit operation. Even within certain resistance range, slight change in the short's resistance can drastically change the circuit operation especially in nMOS transistor. The presence of diodes in pMOS transistor reduces this effect. The dependence of circuit operation on the resistance can be demonstrated by considering the case when gate-to-drain is shorted of nMOS transistor. For a particular pulse input, the inverter showed degraded voltage levels for decreasing resistance. To examine the effect of short for the full range of possible resistance values, the output voltage is plotted in fig. 4 based on simulation data for logic 0 (0 V) input. For R between 100 $\text{K}\Omega$ and 4 $\text{K}\Omega$, the logic function of the inverter is correct but degraded after R is smaller than 4 $\text{K}\Omega$.

For p-channel transistor, the most obvious difference is the presence of a p-n junction diode in a gate oxide short. The presence of the diode actually adds an additional resistance and reduces the effect of the short when it is provoked. Simulation results for gate-to-source short of pMOS transistor show that the output voltage does not degrade even at $R = 1 \text{ K}\Omega$ (Fig. 5).

When the diode is reverse-biased, its effect depends on its reverse breakdown voltage, V_{BR} . If V_{BR} is greater than the operating voltage range of the circuit, there is negligible current through the diode, and thus no faulty effects are caused. However, low reverse breakdown voltages of about 1-2 V were observed for some gate-to-channel shorts in n-channel transistors (Hawkins and Soden, 1985; Segura *et al.*, 1991). Low breakdown voltage can also occur for gate-to-source and gate-to-drain shorts and these soft breakdowns also produce large resistances (Hao and McCluskey, 1993). As a result, the presence of the diode significantly reduces the effect of the shorts.

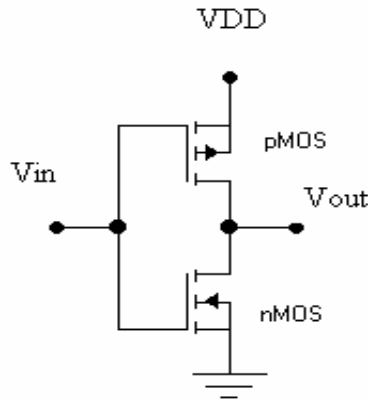


Fig. 3. A CMOS inverter.

Table 1. Change in output voltage due to the variation of power supply.

Resistance (R)	V_{DD} (V)	V_{out} for gate-to-source short (Volts)	V_{out} for gate-to-drain short (Volts)
10 $\text{K}\Omega$	5	5	4.4
	4	4	3.5
	3	3	2.5
5 $\text{K}\Omega$	5	5	3.6
	4	4	3.1
	3	3	1.8

(ii) Effect of supply voltage: In n-channel transistor, a high power supply reduces and a low power supply enhances the effect of gate oxide short. By keeping the short resistance in a particular value, power supply (V_{DD}) is varied. Simulation results have been summarized in table 1 for $R = 10\text{ K}\Omega$, $5\text{ K}\Omega$ for nMOS at logic 0 (0 V) input.

The incorrect logic output results when $R = 1\text{ K}\Omega$ (Fig. 6). On a static current path derived by a short, the resistance of the transistor is higher for a lower gate-to-source voltage, V_{GS} .

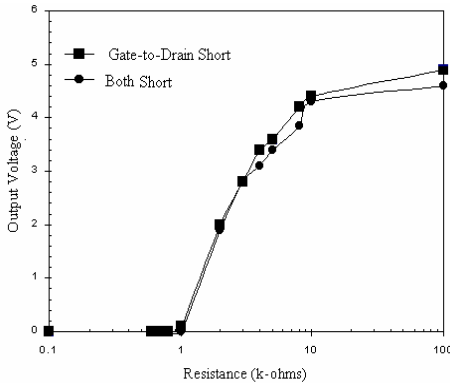


Fig. 4. Effects of gate oxide shorts on output voltage due to the variation of resistances.

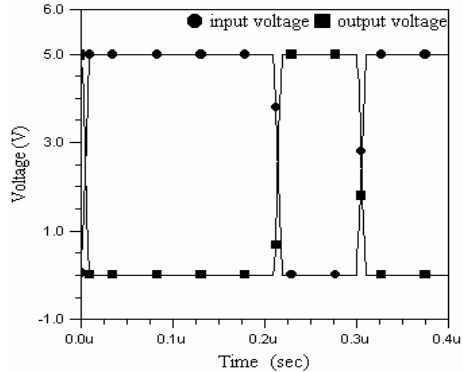


Fig. 5. SPICE simulation result for $R = 1\text{K-ohm}$ (pMOS).

Table 2. Change in output voltage of pMOS transistor due to the variation of power supply at logic 0 (0 V) input.

Resistance (R)	V_{DD} (V)	V_{out} for gate-to-source short (Volts)	V_{out} for gate-to-drain short (Volts)
10 $\text{K}\Omega$	5	5	4.8
	4	4	3.75
	3	3	2.8
5 $\text{K}\Omega$	5	5	4.4
	4	4	3.5
	3	3	2.6
1 $\text{K}\Omega$	5	5	2.9
	4	4	2.3
	3	3	1.8

Since the transistors gates are connected to the logic gate input, a lower V_{DD} means a lower V_{GS} , and thus a higher transistor resistance. Therefore, the relative resistance of the short is lower at a lower V_{DD} , resulting in enhanced faulty effects and vice versa.

For p-channel, when the voltage across the diode decreases, the resistance of a short increases. The effect of such a short would depend on the relative rate of resistance change of the short and of the transistors on the static current path. Simulation results

have been shown in table 2. For reverse biased diode, the faulty effect is unpredictable since the diode's V_{BR} may change as the voltage across the diode changes (Hao and McCluskey, 1993).

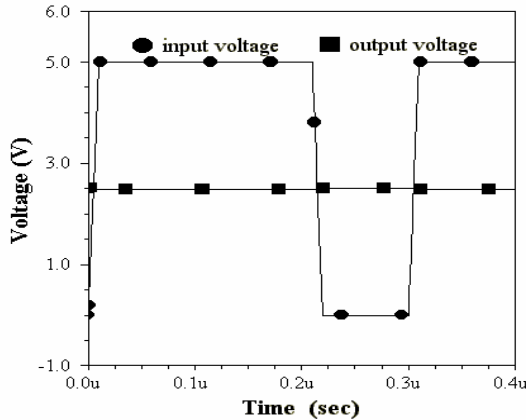


Fig. 6. SPICE simulation result for R =1 K-ohm (nMOS).

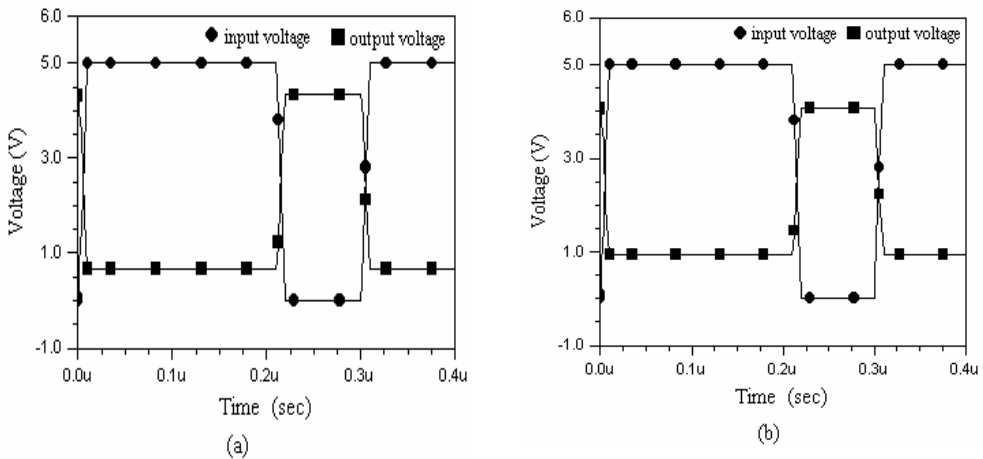


Fig. 7. SPICE simulation results for temperature dependence. (a) T = 27°C, (b) T = 100°C both at R = 5 KΩ.

(iii) Effect of temperature: The temperature dependence is observed in both n- and p-channel transistors. The conductance of a transistor is proportional to the mobility of the carrier, which inversely changes with temperature. So, the relative resistance of a short on a static path is smaller at higher temperature and this enhances the faulty effects. Similarly, the effect is reduced at higher temperature. Fig. 7 confirms this statement for

nMOS transistor. For p-channel transistor, simulation results confirm the marginal effect of gate-to-drain short of pMOS transistor if the temperature changes.

Discussion

Depending on the resistance neither too large nor too small, logic circuit operation can be very sensitive to a small variation in the resistance. Shorts in this region cause marginal circuit operation. Marginally operating circuit due to shorts is vulnerable not only to small variation in a short's resistance but also to the changes in a circuit's operating environment. Even change in power supply or operating temperature can enhance the errors in a logic circuit although that would not occur under normal condition. Various results identify gate oxide shorts to cause production failure (Woods, 1986). This phenomenon makes the circuit vulnerable to device degradation over time and causes circuit failure affecting the reliability of the system or circuit.

Conclusion

A realistic gate oxide short model has implemented to analyze the logic operation of a CMOS inverter. The faulty effects were more pronounced in n-channel transistor compared to p-channel. Variations of power supply and temperature give an idea of the different faulty effects of nMOS and pMOS transistors. Obtained results show the better performance for p-channel transistor due to the presence of a diode in its equivalent circuit. Therefore, the circuit operation strongly depends on the resistance of the gate oxide short and change in power supply and temperature.

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