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MINIMIZATION OF PROPAGATION DELAY OF CMOS INVERTER DRIVING AN RC LOAD

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Abstract: The propagation delay of a signal through resistive network in large chips can limit the circuit performance. In order to develop a repeater design methodology, a complementary metal-oxide-semiconductor (CMOS) inverter driving an *RC* load is presented. By using Sakurai's short channel α-power law model of transistor operation, the inverter model is applied to the problems of repeater in order to determine the reduced delay inserted along a *RC* line. For a typical *RC* load *(R =1K, C =1pF)*, this repeater model exhibits less error as compared to a dynamic circuit simulator (SPICE).

Key words: Repeater; Propagation delay; Saturation conductance; Transistor model

Introduction

Due to the increase in the size of CMOS integrated circuits, interconnections inside the chip become more significant. With a linear increase in length, interconnect delay increases due to linear increase in both interconnected resistance and capacitance. In addition, the large interconnected loads not only affect the performance, but also degrade the wave shape, causing excessive short-circuit power to be dissipated in the stage loading a CMOS logic gate (Douglas, 1985). Several methods have been introduced to reduce the interconnection delay so that these impedances do not dominate the delay of a critical path [Wu et al., 1990]. A timing model of a CMOS inverter driving an *RC* load can be implemented to form the basis for the repeater design methodology which reduces the propagation delay of the signal through inverter.

Inverter Delay

An inverter driving an *RC* load is shown in Fig.1. By using an analytical model (short-channel transistor model), the output voltage of a CMOS inverter can be realized by giving a step input. The α-power law model accurately describes the effects of short-channel transistor behavior such as velocity saturation. In CMOS inverter, the n-channel linear drain current is given by (Sakurai and Newton,1990):

$$C\frac{dV_{out}}{dt} = \frac{I_{do}}{V_{do}}\left(\frac{V_{gs}-V_T}{V_{DD}-V_T}\right)^{\alpha} V_{ds} \qquad (1)$$

for $V_{gs} \geq V_T$, $V_{gs} - V_T \geq V_{ds}$.

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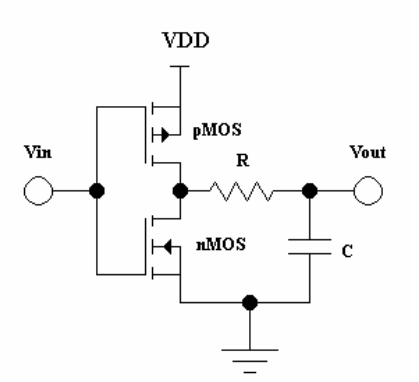

Fig. 1 A CMOS inverter driving an *RC* load.

In the α-power law model, I_{do} represents the drive current of the MOS device, V_{do} represents the drain-to-source voltage at which velocity saturation occurs with $V_{gs} = V_{DD}$ and α models the process dependent degree to which velocity saturation affects the drain-to-source current. α is within the range $1 \le \alpha \le 2$ where $\alpha = 1$ corresponds to a device operating strongly under velocity saturation, while $\alpha = 2$ represents a device with negligible velocity saturation. V_{DD} is the supply voltage, and V_T is the MOS threshold voltage (Sakurai et al., 1990). Assuming a step input is applied to the circuit shown in the Fig.1. The analysis shows that

$$V_{out}(t) = V_{out}(0)exp[-g_{do}t/(g_{do}RC + C)] \quad (2)$$

where saturation conductance, $g_{do} = I_{do}/V_{do}$.

The expression for V_{out} can be rearranged to determine the time required for a CMOS inverter to reach an output voltage V_{out} giving a step input signal:

$$t_{out} = \frac{g_{do} RC + C}{g_{do}} \ln(V_{DD} / V_{out}) \quad (3)$$

The above expression is used to express the 50% and 90% output delay with respect to a step-input signal. These time delays are:

$$t_{50} = 0.693 \frac{(1 + g_{do} R_{int}) C_{int}}{g_{do}} \quad (4)$$

and,

$$t_{90} = 2.3 \frac{(1 + g_{do} R_{int}) C_{int}}{g_{do}} \quad (5)$$

These expressions are used to model the total delay required by a repeater chain to drive an *RC* load (Debnath et al., 1999).

Delay of a Repeater Chain Driving an *RC* Load

The delay required to propagate a signal through a highly resistive interconnect can be reduced if the interconnect is broken up and distributed among a number of repeaters (Fig. 2). The total time delay t_{total} from the input to the output of an n-stage repeater system is given by

$$t_{total} = t_{first\ stage} + (n-2)\, t_{int.\ stage} + t_{final\ stage} \quad (6)$$

The first component of $t_{first\ stage}$ is the time required for the output signal of the first repeater to drop from V_{DD} to V_{TN}, the threshold voltage of the n-channel device assuming a step input signal.. It is also assumed that the rising (falling) output of an inverting repeater reaches V_{TN}

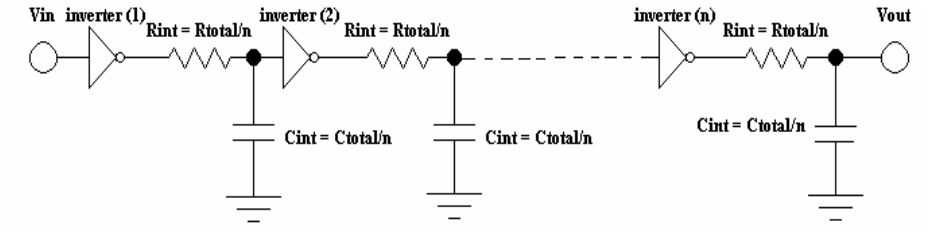

Fig. 2. n equal sized CMOS inverting repeaters driving an RC load.

$(V_{DD}+V_{TP})$ by the time the falling input reaches V_{TN} $(V_{DD}+V_{TP})$. Hence, the signals waveforms of the intermediate stages consistently operate between $(V_{DD} + V_{TP})$ and V_{TN}. The delay for each successive stage, $(n-2)t_{int.\ stage}$, excluding the final stage, is modeled as the time required for the signal to transition from $V_{DD} + V_{TP}$ to $V_{TN.}$ For the rising repeater output, intermediate delay is given by (Adler et al., 1998)

$$t_N = \frac{(1 + g_{do} R_{\text{int}}) C_{\text{int}}}{g_{do}} \ln[(V_{DD} + V_{TP}) / V_{TN}] \qquad (7)$$

For falling repeater output delay (t_P), similar expression is found (Adler et al., 1998).

Results

In order to determine the total delay to the 90% point, $t_{final\ stage}$ is t_{90} given by equation (7). t_{90} is compared with analytic total delay (table 1). A plot of t_{90} (90% output delay time) versus the number of the repeater stages (n) for an *RC* load of *1K* and *1pF* is shown in fig.3.

Table 1. Comparison between Total Delay model (*90%* output delay) and AIM-SPICE for *R*=1K, *C*=1pF.

No. of stages	Analytic (ns)	AIM-SPICE (ns)
1	5	4.04
2	2.5	2.56
3	2.2	2.1
4	1.8	1.839
5	1.7	1.67
6	1.61	1.622
7	1.58	1.564
8	1.52	1.519
9	1.50	1.482
10	1.47	1.448

From fig. (3), it is found that the delay decreases as no. of stages increases but complexity of the circuit increases. Therefore, an optimum number of repeater stages can be taken to be eight, after that delay does not reduce significantly.

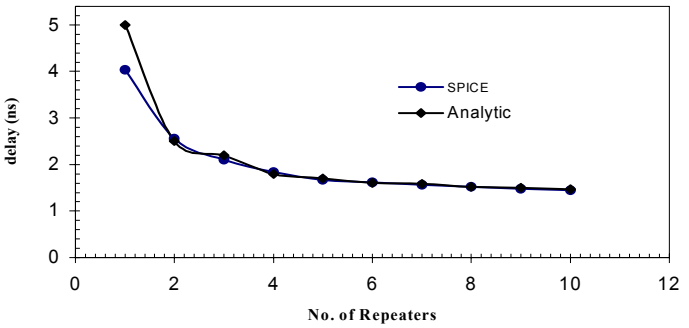

Fig. 3. Total delay (t_{90}) as a function of no. of repeaters.

t_{90} for different repeater sizes is summarized in table 2. These are derived using SPICE.

Table 2. t_{90} versus repeater width using SPICE (*0.8 μm* technology).

Repeater width (μm)	t_{90} (ns)
1	15
3	5
5	3.2
7	2.2
10	1.67
12	1.48
15	1.2
18	1.05
20	0.98
25	0.8
30	0.7

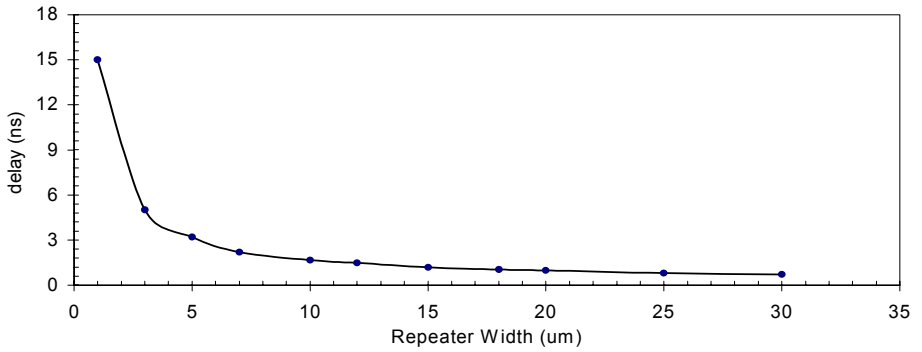

Fig.4 Total Delay time in various repeater width (w).

The delay versus repeater width is plotted in Fig.4. From the figure, the repeater width can be taken to be 16 μm. In this repeater design methodology, the following values have been taken into account:

Width of the MOSFETs, $W = 10$ μm.
Channel length, $L = 0.8$ μm.
Threshold voltage, $V_{TN} = 0.844$ V *(nMOS).*
Threshold voltage, $V_{TP} = -0.735$ V *(pMOS).*

Discussion

The CMOS inverter model driving a resistance and capacitive load reduces the propagation delay leaving a maximum error of 24% as compared to SPICE. It is found that the delay decreases as the number of repeater stage increases, but it also leads to circuit complexity. Therefore, an optimal number of repeaters can be taken to be eight. Also, with the increase of the size of the repeaters the delay decreases and attains almost a constant value for large size of repeaters. The delay decreases drastically up to ten repeaters but after that the delay reduces slowly. Increasing the size of the repeater reduces the delay, but it also degrades the device parameters. So there is a need to optimize the size of the repeaters. The optimum size of the repeater calculated from the graph comes out to be 16 μm.

Conclusion

CMOS inverters driving an *RC* load have been discussed based on α-power law device model. This timing model has been expanded to determine the overall delay of a signal propagating through a uniform repeater chain driving large distributed RC load. Analytical estimate of delay with the design equations are within 24% error compared to SPICE for long resistive interconnect. Therefore, inserting repeaters in *RC* line can greatly improve the signal delay characteristics.

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